

REMARKS/ARGUMENTS

Claims 1, 2, 5-11, and 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirsch et al. (US Patent No. 5,566,326) in view of Macera et al. (US Patent No. 5,490,252). Claims 3, 4, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirsch et al. and Macera et al. further in view of Hamilton, II et al. (US Patent No. 6,633,977).

Joint Inventorship

In response to the Examiner's comments regarding joint inventorship, Applicants submit that the inventors of the present application have not changed. The inventors remain to be Hui-Lin Li and Bahar E. Baran. Copies of both signature pages of the declaration under 37 C.F.R. § 1.131 as signed by the inventors are attached.

Claim 1

Applicants respectfully traverse the rejection of claim 1 under §103(a). First, the cited references Hirche et al. and Macera et al. cannot be properly combined. Second, even if combined, the combination of Hirsche et al. and Macera et al. still fails to disclose all of the recited features of claim 1. For these reasons, which are discussed in detail below, claim 1 is patentable over these two references.

I. Hirche et al. and Macera et al. cannot be combined

First, Hirche et al. and Macera et al. cannot be properly combined. Neither Hirche et al. nor Macera et al. contains any motivation for combining these two references together. The Examiner certainly does not identify any such motivation. See Office Action dated 8/28/06. Indeed, Hirche et al. and Macera et al. disclose non-analogous technology areas that do not seem to have any connection to one another.

Hirche et al. is directed to a technique for software emulation. See e.g., Hirche et al., Figs. 1a and 1b, col. 1, lines 36-38 and col. 3, lines 40-56. As is known in the art, an emulated system typically refers to a computer software program that was originally written for another system and not the host system. However, for whatever reason, the computer software program needs to be "emulated" within the environment of the host system. An example of such

an arrangement is a personal computer (host system) that is used to emulate an arcade video game (emulated system) that was originally written not for the personal computer, but for an arcade video game console. As disclosed in Hirche et al. and as well known in the art, the host system may comprise I/O devices. See Hirche et al., Fig. 1b, reference number 58c. For example, such I/O devices may include a mouse, a joystick, etc.

Macera et al. is directed to a technique for packet switching. In particular, a special switch device referred to as the Broadband Enterprise Switch (BES) receives a packet of a particular native format -- e.g., Ethernet -- from a network, converts the packet into the "internal packet format," performs the necessary switching, then converts the packet from the "internal packet format" to another native format -- e.g., Token Ring -- before delivering the packet to another network. The benefit of this technique is that switching of packets is always performed in the "internal packet format," which make the resources-intensive switching process more "normalized" and therefore more efficient. See e.g., Macera et al., Fig. 3 and col. 6, lines 29-47.

There is absolutely no motivation for combining Hirche et al. and Macera et al. The emulation technique of Hirche et al. does not find any applicable use in the packet switching technique of Macera et al. Clearly, there isn't any need for packet switching devices to emulate a software program. Similarly, the packet switching technique of Marcera et al. does not find any applicable use in the emulation technique of Hirche et al. Software emulation as taught by Hirche et al. is performed completely in software internal to a host system and has no need for conducting any packet switching.

In fact, there is specific teaching away from combining these two references. Macera et al. explicitly teaches against applying its packet switching techniques in a microprocessor-based environment, which is considered prohibitively time-consuming. See Macera et al., col. 5, lines 57-63. Yet a microprocessor environment is exactly what Hirche et al. requires. The host system of Hirche et al. must include a microprocessor that carries out the operating system level and user system level constructs which make up the emulated version of a software program. See Hirche et al., Fig. 1a, reference numbers 64 ("Operating System Level"), 62 ("User Level"), and 58a ("CPU").

Thus, not only is there no motivation for combining Hirche et al. with Macera et al., there is specific teaching away from combining these references. Consequently, Hirche et al. and Macera et al. cannot be combined as proposed by the Examiner.

II. Even if combined, the combination of Hirche et al. and Macera et al. fail to disclose all of the limitations of claim 1

Even if combined, the combination of Hirche et al. and Macera et al. fail to disclose all of the limitations of claim 1. Claim 1 requires the step of:

"Translating data for the circuit related objects from binary data to ASCII data in the network control processor"

The Examiner acknowledges that Hirche et al. fails to disclose translating data for the circuit related objects from binary data to ASCII data in the network control processor. However, the Examiner alleges that Macera et al. performs this step. This is an incorrect for at least two reasons.

First, Macera et al. simply does not translate binary data to ASCII data, period. The portion of Macera et al. cited by the Examiner describes the conversion of packet formats, e.g., from a native packet format such as Ethernet to an "internal packet format." See Office Action dated 8/28/06, citing Macera et al., col. 6, lines 38-42. However, this has nothing to do with translation of binary data to ASCII data. As is well known in the field of network technology, a packet format does not inquire into the contents of its payload. In other words, a packet format is only responsible for delivering its payload of data; the packet format does not care whether the contents of the payload is interpreted as binary data or ASCII data. Thus, the conversion of a packet from one packet format to another packet format does NOT involve any change to the payload itself. Thus, the conversion of packet format as taught by Macera et al. does not involve any translation from binary data to ASCII data. To do so would alter the contents of the payload of the packet, which is clearly not intended by Macera et al. or any other known network switching device for that matter.

Second, the conversion of one packet format to another packet format cannot be substituted for the translation of binary data to ASCII data. These are completely different processes that are used for different purposes. One cannot simply remove the translation of

binary data to ASCII data and in its place insert the conversion of one packet format to another packet format. Thus, it is clear that even if combined, the combination of Hirche et al. and Macera et al. would still fail to disclose all of the limitations of claim 1. For at least the reasons stated above, Applicants submit that claim 1 is patentable over Hirche et al. and Macera et. al.

Claims 10 and 19

Claims 10 and 19 are each rejected on similar rationale as that for claim 1. For at least the reasons discussed above with respect to claim 1, claims 10 and 19 are also patentable.

Claims 2-9 and 11-18

Claims 2-9 and 11-18 depend from claims 1 and 10, respectively, and incorporate all of the limitations of their corresponding base claims. For at least the reasons discussed above with respect to claims 1 and 10, claims 2-9 and 11-18 are also patentable over Hirche et al. and Macera et. al.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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